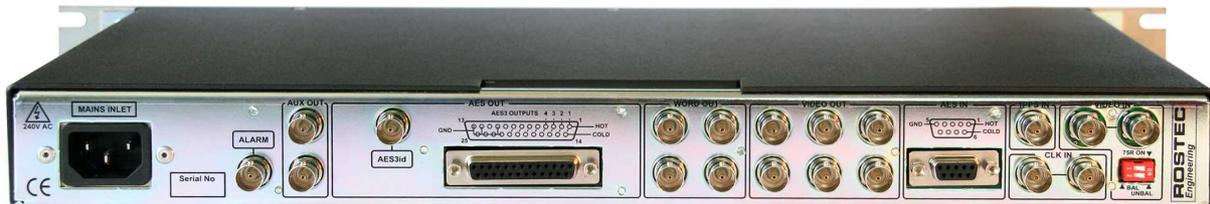
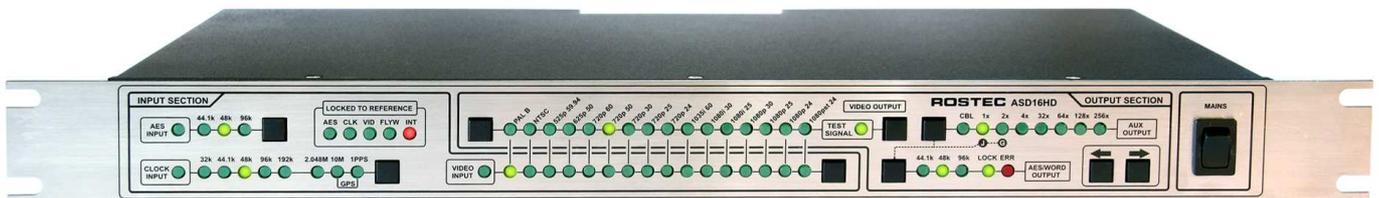


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ASD16HD Reference Generator



ROSTEC ASD16HD Reference Generator

Revision 9

(Updated to UL product mark specification)

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ASD16HD Reference Generator

Features

- HD video tri-level sync: 1080p, 1080i, 1035i, 720p, compliant with SMPTE 274M, 240M and 296M
- SD video output: PAL 25 Hz or NTSC 29.97 Hz
- Test pattern generator, PAL and NTSC Color Bar, HD hatch pattern.
- AES3 output @ 44.1, 48 and 96 kHz
- AES3id output @44.1, 48 and 96 kHz
- Word output: 44,1, 48, 96 kHz
- AUX output: Word x2, x4, x32, x64 x128 x 256, CBL
- Internal reference based on Oven Crystal Oscillator. Accuracy 0.2 ppm ($0.2 \times 10E-6$), 0 – +50 deg.C
- HD and SD video sync input accepts bi-level and tri-level sync input. 16 different video sync input formats are supported.
- AES sync input @ 44.1, 48, 96 kHz.
- Word/clock sync input supports GPS 10 MHz/1PPS
- Extensive interoperability between sync inputs and sync outputs (see Appendix section)
- Automatic delay calculation ensures correct alignment between video frame/AES block/Word edge/1PPS for any chosen input/output combination.
- The video odd/even alignment for interlaced formats is maintained, even with different video input/output formats.
- Extreme sync safety. Active “de-bouncing” of inputs by means of a high performance input detector and a built in precision fly-wheel.
- Switching between sync inputs and the internal reference is performed by a soft glide function.
- Easy operation and easy status readability via the no-nonsense front layout.
- Glide mode and input de-bouncing efficiently absorbs sync drop-outs
- Excellent jitter and wander specifications.
- Linear low noise power supply
- Sturdy steel metal sheet casing.
- Affordable price.

General description

The ASD16HD is a high performance, high precision Digital Reference Generator designed to operate as master or as slave in a video/audio studio environment. It generates 16 different SD and HD video sync output formats, and 44.1 kHz, 48 kHz and 96 kHz AES3 digital audio outputs and Word Clock outputs. It features an AUX output that functions as a Word clock multiplier, supporting up to 256 times the sample rate frequency, thus being able to output various non-standard clocks (like f. ex. Pro-Tools super clock).

The ASD16HD is able to synchronize to an extensive range of input signals. It can lock the outputs to sixteen formats of incoming video sync, three AES sampling frequencies and eight clock frequencies. It has the ability to align the video output frame to the 1PPS GPS pulse. A video interlaced format will align the first frame (odd frame) to the 1PPS leading edge. A video progressive format will align any frame. The 1PPS only works together with the 10 MHz input. Both signals must come from the same GPS receiver. Observe that not all video formats are suited for this kind of synchronization (see Appendix section).

The ASD16HD has an extensive ability to bridge sync formats across various platforms. Whenever an integer relationship exists between the input and output Frame/AES block/Clock edges, the generator will lock the incoming and outgoing signals in perfect position sync.

A separate processor calculates and applies the necessary time delay for the various formats to align edge to edge within one master clock pulse. The circuit keeps track of odd/even frames in interlaced formats, and it is able to synchronize the incoming odd/even frame to the outgoing odd/even frames in interlaced formats, even if the formats are basically different. The only requisite is an identical frame rate for the input and output (see Appendix for a list of possible formats).

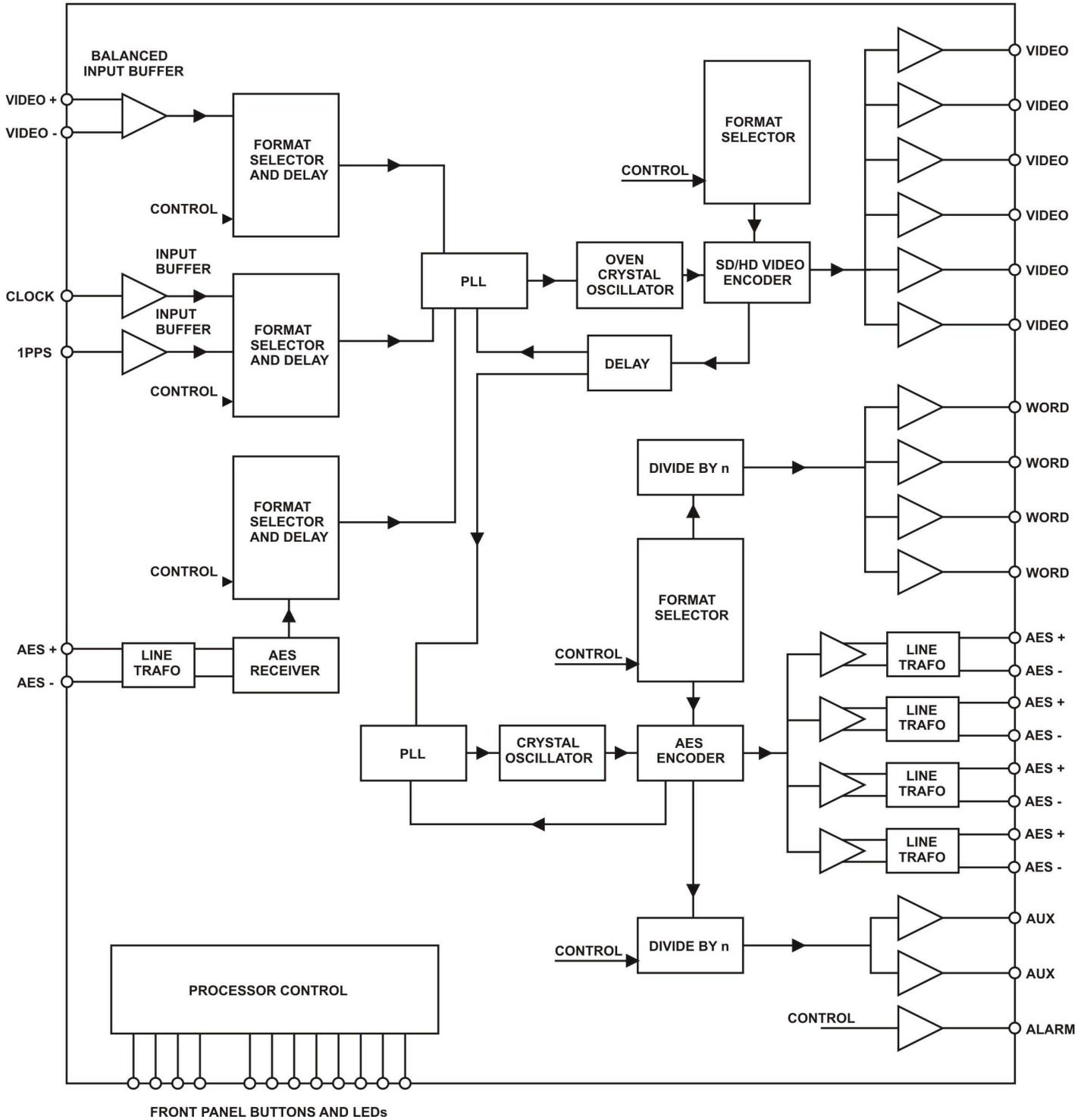
If the input AES/Clock frequency and the video output frame rate have no simple mathematical relationship, the generator will still be able to lock. The lock will not be a position lock, but it will be a perfect frequency lock. Input frequency accuracy is transferred directly to output frequency accuracy, even when the basic frequencies are different.

The input locking mechanism is based upon an extensive sync safety philosophy. The circuit performs input “de-bouncing” which efficiently absorbs sync dropouts by means of an intelligent fast reacting input detector, a high precision flywheel and a unique glide principle.

The AES/Word/AUX outputs are always locked to the video sync output. When an integer relationship between frame and AES/Word/AUX frequency exists, the ASD16HD generator keeps a perfect positional relationship between video frame start, AES block start and Word/AUX leading edge.

ASD16HD Reference Generator

Simplified Functional Schematic



ASD16HD Reference Generator

Signal flow

The heart of the ASD16HD is a high grade crystal oscillator built into a temperature controlled oven together with all the necessary voltage references and regulators for its operation.

This scheme results in excellent frequency stability over the specified temperature range, far superior to a standard temperature compensated crystal oscillator. The frequency accuracy is better than 0.2 ppm from 0 to +50 C. ($0.2 \times 10E-6$)

The factory adjustment is typically 0.1 ppm at 25 C.

The ASD16HD **always** uses this oscillator as the central source for all Video, AES, Word and AUX outputs, no matter whether the generator runs on its own or if it is locked to an external sync source.

When the generator locks to an external sync, it simply tunes the internal crystal oscillator to mirror the frequency of the incoming reference. At the same time the position relationship between the incoming and outgoing signal format is calculated, and the necessary delay is applied to the sync mechanism. The generator does not jump to this delay setting; it glides softly until a perfect position lock is achieved, and while it is gliding, it continues to supply uninterrupted sync.

The scheme ensures the correct frequency and position relationship between incoming sync and outgoing sync, as recommended in the relevant standards.

A separate AES encoder circuit generates the AES, Word and AUX signals. The local crystal oscillator that feeds the AES encoder is permanently locked to the video encoder by means of a high precision low jitter phase locked loop.

In the same manner as the input circuit, the position relationship between the video and the AES/Word/AUX signal format is calculated, and the necessary delay is applied to the sync mechanism.

Thus, no matter which video output format is selected, and no matter which AES/Word/AUX format is selected, the timing relationship between the Video, AES, word and AUX outputs is never broken apart, and the result is that all outputs are in perfect and correct sync.

Note: Some signal formats have a mathematical relationship that makes position synchronization between frame/block boundaries impossible. When synchronization of such signals is chosen, frequency synchronization is applied

See Appendix for a comprehensive list.

The ASD16HD is built with extreme sync safety in mind. It always uses the internal oscillator as the master clock for all generated output signals.

When it runs as a stand alone generator, it uses the built in reference to keep the output frequency accurate.

When it locks to an incoming reference, it continues to use the internal oscillator as the master clock, but gently adjust the oscillator frequency to match the frequency of the incoming signal, creating a phase lock between input and output.

When the incoming signal is lost or discontinued, the generator uses the internal flywheel to keep the oscillator running at the last good frequency as if nothing has happened.

If the incoming signal has not returned within a specified time period, the master clock oscillator gently glides back to its internal reference, and the generator continues to generate sync signals without disruption. If the incoming signal returns before the specified time-out, the oscillator gently glides into phase lock with the incoming signal, re-establishing the correct time relationship between input and output.

When the master clock oscillator glides back and forth between sources, the generator continues to deliver sync outputs without gaps or disturbances.

Input detector and Flywheel

To take full advantage of glide mode, the ASD16HD uses a combination of an efficient input detector and a high precision flywheel.

The input detector is fast, intelligent and rather brutal. It looks at the leading edges of the incoming signal, and based on the incoming frequency, it calculates the expected position of the next incoming pulse and sets up a narrow window, inside which every subsequent leading edge must fall. If any leading edge falls outside this window by more than 100 nsec, the input signal is immediately rejected.

When this happens, control is instantly handed over to the flywheel, ensuring that the master clock continues to run at exactly the same frequency. Thus the generator keeps the same output sync position, while it is waiting for the incoming sync to return.

In order for the input signal to be accepted again, 128 consecutive leading edges must fall inside the window of acceptance. Only then is the input signal routed to the Phase Lock Loop circuit. The master oscillator will then gently glide into phase lock, softly compensating for any accumulated time difference.

The clock input needs 128 consecutive good pulses
The video input needs 128 line pulses.

ASD16HD Reference Generator

The 1PPS input needs 3 pulses

The AES input needs 192 frames AND no bi-phase violation of the Manchester code during one AES block.

The scheme is extremely efficient, when it comes to catching disruptions of the incoming sync, caused by a faulty connector or cable. It works much in the same way as the de-bouncing circuit applied to pushbuttons in digital control systems, only in this situation the de-bouncing is performed on the incoming sync signal.

In fact, the de-bouncing is so efficient that a faulty installation often will pass unnoticed, simply because the generator continues to smoothly generate syncs, while it uses its flywheel to elegantly skip over the gaps and interruptions of the incoming sync signal.

To assist technical personnel in diagnosing a faulty installation, an alarm output is available on the back panel. The alarm is a TTL output, which goes low for a brief period of time whenever the incoming sync is rejected by the input detector.

Jump mode vs. glide mode, input section

Glide mode is extremely efficient when it comes to compensate for sync drop outs, f. ex. in case of a faulty wire or an intermittent connection. The reason is that when the sync drops out it usually returns with the same timing except for a small drift due to differences in reference frequencies of the ASD816HD and the connected unit.

When the ASD16HD again locks to the incoming sync, the accumulated time difference is quite easily compensated for by the ASD16HDs oscillator. It simply glides gently into phase lock and the incident will normally pass unnoticed (except for an Alarm indication)

There are instances where this is not the case. If the external unit that generates the incoming sync is switched on and off, the time difference can be any value between zero and half a cycle of the incoming sync. When the sync source is Video or GPS 1PPS it is simply not acceptable to wait for the oscillator to catch up in glide mode.

To overcome this, the ASD16HD automatically switches to jump mode when the time difference is bigger than a preset value, set by software to 300 usec.

The ASD816HD will jump into coarse sync and make the last fine correction in glide mode.

When the input is a Clock signal, the generator will always glide into sync. Normally it will only take a couple of seconds for the generator to achieve sync.

When the input is an AES signal, the generator will also always glide into sync.

When the input is a 44.1 kHz AES signal, the generator automatically switches to clock mode.

The reason is that 44.1 kHz is an odd-ball in the whole synchronization scheme. The block size and time length of a 44.1 kHz AES signal does not fit into any video frame, neither SD nor HD. The only useful sync signal that can be extracted from the 44.1 kHz AES stream is the word clock, hence the automatic switching to clock mode.

When the input is a 48 or 96 kHz AES signal, the block size has a much more useful size and time length.

The generator extracts the block start (Z-preamble) and uses this as the reference point for synchronization.

The consequence is a slow lock. The glide time when achieving lock can be up to 30 seconds worst case.

Jump mode vs. glide mode, AES output section

The AES/Word/Aux output signals are always locked to the Video sync output signal. The sync lock mechanism has two distinct modes of operation.

In the AES jump mode, whenever a video or 1PPS jump is performed, all output signals jump, including the AES/Word/Aux output

This enables the generator to quickly achieve phase lock between its Video output and its AES/Word/Aux outputs, thus achieving correct timing between the Video sync and the AES/ Word/AUX outputs in a matter of seconds. This is the default mode.

In the AES glide mode, whenever a video sync or 1PPS jump is performed *only the Video sync output jumps*.

The AES, Word and AUX outputs glides to catch up on the Video frame. In this mode the generator is slow to achieve phase lock, *but the AES/Word/Aux outputs are not interrupted when the generator jumps!*

The mode is advantageous in installation where a continuous AES/Word sync signal is necessary even when the input video sync comes and goes and often returns with wildly different timing.

On the front panel it is possible to switch between AES Jump mode and AES Glide mode by pressing the AUX and AES/Word switches simultaneously and changing the status with the arrow switches (see front panel layout).

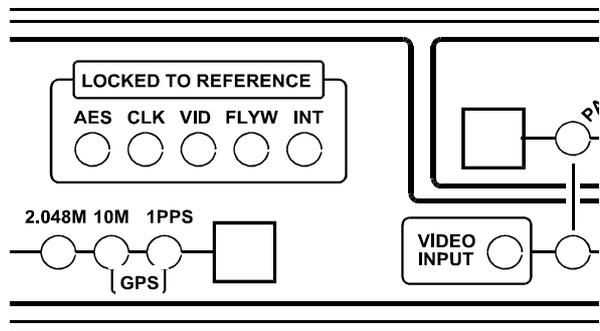
ASD16HD Reference Generator

Selecting an input

There is no manually operated input selector. The input selection is automatic. When the ASD16HD senses an input, it checks certain critical parameters of the signal before switching the input on. If more than one input is connected, the circuit selects the active input by priority.

The order of priority is:

1. Video
2. Clock
3. AES
4. Flywheel
5. Internal Reference



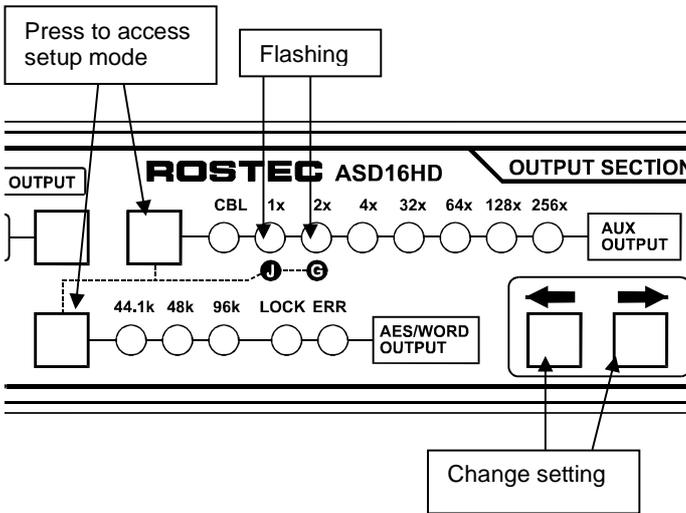
When Video, Clock and AES input signals are connected at the same time, the auto switching mechanism further increases the sync safety. The generator selects the input of the highest priority as the source. If this input drops out, the next in line is selected. If a higher priority input signal returns the generator automatically selects this as the source.

The switching between input sources is done by gently gliding back and forth into correct sync. When the Video, Clock and AES exhibit a correct positional relationship, the switching may go totally unnoticed with an insignificant output frequency change, possibly down to just a fraction of 1 ppm.

If the Video input returns with a time difference larger than 0.3 msec, the generator jumps. The Clock and AES always glides into sync lock.

The 1PPS (1 Pulse Per Second) signal only works together with the 10 MHz clock as part of the GPS synchronization. It is not part of the auto switching scheme.

Each input has multiple settings of frequency and format. To change a setting, press and hold down the relevant input button, and change the setting with the arrow buttons (see front panel layout).



The setup can be accessed and changed on the fly without interrupting the AES and Word outputs.
Note: the AUX outputs are unavailable during the brief moment setup mode is being accessed.

Selecting an output

All outputs are always active and they all have multiple settings of frequency and format.

To change a setting, press and hold down the relevant output button, and change the setting with the arrow buttons (see front panel layout)

Note that changing the AES sampling frequency also changes the Word and AUX frequencies.

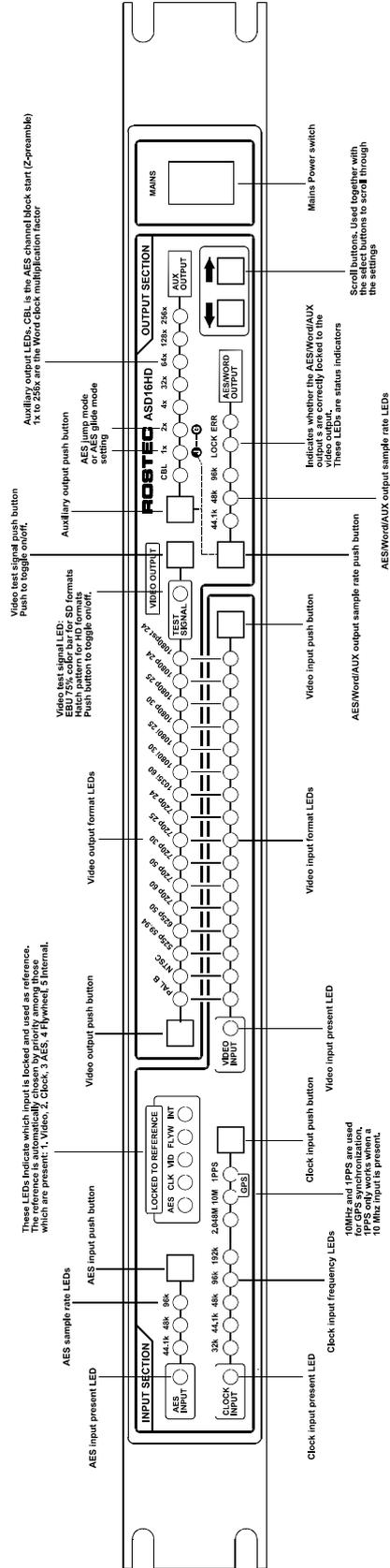
AES sampling frequency and Word frequency are always identical.

The AUX frequencies are simply multiples of the Word frequency.

The CBL is the start of the AES block, thus it also follows the AES sampling frequency

ASD16HD Reference Generator

Front Panel Quick Guide



ASD16HD Reference Generator

FRONT PANEL BUTTONS AND INDICATORS

OBS: Push the buttons firmly and slowly!

----- INPUT SECTION -----

AES input present LED

This LED indicates that an AES signal is present at the input. The signal is accepted when 128 consecutive bits have passed without bi-phase coding violation AND the AES frame structure is correct.

44.1k, 48k and 96 kHz LEDs

These LEDs indicate the selected sample rate for the AES input. The sample rate is manually selected. It is not automatically detected.

AES input push button

This button enables the AES input sample rate to be selected. Press the button, hold it down and select the sample rate with the scroll buttons.

Clock input present LED

This LED indicates that a clock signal is present at the input. The signal is accepted when 128 consecutive leading edges fall inside a predetermined time window. The window is calculated on the basis of the selected clock input frequency.

Note that a 1PPS signal will not activate this LED.

Clock input frequency LEDs

These LEDs indicate the selected frequency for the Clock input. The frequency is manually selected. It is not automatically detected.

The 1PPS will light up when a 1PPS signal is present. The 10 kHz and the 1PPS signals must both come from the *same* GPS receiver for correct time alignment of the 1PPS leading edge and the Video Frame start.

Note: Although the 1PPS sync function is intended to operate with the 10 MHz clock, it actually works with all the other clock formats as long as the input frequency and the 1PPS are time related.

Clock input push button

This button enables the Clock signal frequency to be selected. Press the button, hold it down and select the frequency with the scroll buttons.

Note that 1PPS cannot be selected. It is controlled by the 1PPS input detector.

Video input present LED

This LED indicates that a video sync signal is present. Acceptable formats are all the video sync formats listed on the front plate above the Video format LEDs.

Color subcarrier from PAL and NTSC or color information from HD formats is not necessary.

Note that the generator will only lock to the incoming video sync if the incoming and outgoing frame rates are identical (see Appendix for list).

Video input format LEDs

These LEDs indicate the selected format for the Video sync input. The format is manually selected. It is not automatically detected.

Video input push button

This button enables the Video sync input format to be selected. Press the button, hold it down and select the format with the scroll buttons.

Locked to reference

These 5 LEDs are status indicators for the input phase locked loop.

The AES, CLK and VID light up when the corresponding input is used as reference. Note that these LEDs only light up when the input signal has been accepted AND a phase lock has been achieved.

The Flywheel LED lights up for a few seconds, when the input signal has been lost, after having been used by the generator as the reference.

The INT LED lights up when the generator runs on its internal reference.

If none of the LEDs light up, it indicates that the generator is searching for a valid reference. If this condition lasts for more than a 10-12 seconds, a non-valid input format or frequency may have been selected. If case of a non valid video sync format, the video and flywheel LEDs are flashing. (see Appendix for list).

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----- OUTPUT SECTION -----

Video output push button

This button enables the Video sync output format to be selected. Press the button, hold it down and select the format with the scroll buttons

Video output format LEDs

These LEDs indicate the selected format for the Video sync output. The format is manually selected by using the Video output push button.

Video test signal LED

This LED lights up when the Video test signal is switched on. The test signal is injected directly into the video output signal.

The SD test signal for PAL and NTSC is an EBU 75% color bar. The HD test signal is a standard Hatch pattern, which will generate a square grid pattern on a monitor.

These test signals are only meant as a diagnostics tools for technical personnel.

Video test signal push button

This button toggles the test pattern on and off. It does not work with the scroll buttons.

AES/Word/AUX output sample rate push button

This button enables the sample rate of the AES, Word and AUX outputs to be selected. Press the button, hold it down and select the sample rate with the scroll buttons.

AES/Word/AUX sample rate LEDs

These LEDs indicate the selected sample rate for the AES, Word and AUX outputs.

Lock/Error

The Lock LED indicates that the AES, Word and AUX outputs are phase locked correctly to the Video output via the internal PLL. This LED should light up during normal operation.

The ERR LED indicates that the AES, Word and AUX outputs have broken free of the Video output. It will light up for a few seconds when the unit is powered up, and it will light up briefly when output sample rate frequency is changed or when the video generator

performs a time jump. It should be off during normal operation. These two LEDs are status indicators.

Note that the ERR LED may light up considerably longer when the AES output section is set to glide mode. When a video or 1PPS time jump is performed the AES section will glide into sync with the new video frame position after the jump. During this time the ERR led will light up, worst case can be up to 40 seconds. This is perfectly normal and just a consequence of the chosen mode.

AUX output push button

This button enables the AUX output multiplication factor to be selected. Press the button, hold it down and select the setting with the scroll buttons.

AUX output LEDs

These LEDs indicate the selected multiplication factor or CBL signal for the AUX outputs.

1x to 256x multiplies the Word clock. For example, if 48 kHz sample rate is selected and 256x multiplication factor is selected, the AUX output will be a 12.288 MHz clock (which happens to be pro-tools super clock, btw) CBL is the Channel Status Block Start of the AES signal (the Z-preamble). This signal is handy for testing and diagnostics. It is mostly used in connection with installation service and lab work.

Scroll buttons

These buttons are used to change settings of the inputs and outputs.

AES jump mode and glide mode setting

It is possible to switch between AES Jump mode and AES Glide mode by pressing the AUX and AES/Word switches simultaneously and changing the status with the scroll buttons.

The AUX 1x and 2x LEDs will indicate the selected mode when the AUX and AES/Word switches are held down simultaneously.

This is the only hidden setting on the generator.

Power Switch

The switch turns main power on and off

ASD16HD Reference Generator

There are no special considerations to observe when powering up the unit. Allow a warm up period of 5 minutes to let the internal oven crystal reference settle to its 0.2 ppm absolute frequency precision. If an external reference is connected to any of the generators inputs

upon start up, the generator will immediately be able to achieve lock, as long as the incoming reference is better than +/-25 ppm in absolute frequency precision.

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Back Panel Connections

Video input

The video input circuit consists of a balanced input buffer configuration. The center pin of the BNC connector is the positive input and the ring is the negative input. Normal mode and balanced mode can be selected by the slide switch beneath the two video connectors. In normal mode (unbalanced) the ring is connected to ground.

OBS: Leave the switch in normal position if the video input is not used. Otherwise touching the ring of the video input connector may cause false triggering of the video input circuit.

The input is not internally terminated, and the two input connectors are configured as loop thru, allowing for a serial chain configuration with a single 75 Ohms termination at the end of the chain.

75 Ohms termination can be selected by the slide switch beneath the two video connectors.

Always make sure the video input signal is terminated by 75 Ohms. This is particularly important for SD video like PAL and NTSC. Failure to do so will result in a small time shift of 50-80 nsec between Video input and Video output of the generator.

The reason is that these old formats have bandwidth limitations that in effect create a sloping leading edge on all sync pulses, thus translating amplitude variations to time shift.

The video input accepts SD video bi-level sync and HD video tri-level sync with amplitudes ranging from 0.15 to 2.0 V. In balanced mode the input amplitude + the common mode voltage must not exceed 5.0 Volts

The ASD16HD will lock to a range of SD and HD video sync signals, interlaced formats as well as progressive scan formats. The various formats can be selected by the push buttons on the front panel. A description of all valid sync input formats can be found in the Appendix.

Note: The SD video lock mechanism is a frame lock. It does not provide a color sub carrier phase lock and thus does not perform a PAL-4 or a PAL-8 phase lock between input video and output video.

Clock input

The Clock input is unbalanced and has a nominal sensitivity of 0.5 V. Max level is 10V, AC all well as DC. The input circuit consists of a Schmitt trigger and pulse shaper, making the input compatible with both square wave and sine wave signals.

The input is not internally terminated, and the two input connectors are configured as loop thru, allowing for a serial chain configuration with a single 75 Ohms termination at the end of the chain.

The input accepts a range of standard frequencies, which can be selected by the push buttons on the front panel.

1PPS input and GPS sync

The 1PPS input is TTL compatible, unbalanced, unterminated and 10 kOhms, intended for use with GPS receivers.

The 1PPS works in combination with the 10 MHz signal. Both signals must come from the same GPS receiver.

The two signals provide the positional information and the frequency information necessary to align the video frame to the global time update pulse of the GPS satellite system. When a 10 MHz signal is not used, the 1PPS should be disconnected from the unit.

If the time difference between the 1PPS and the video frame is smaller than approx 300 usec, the ASD16HD will glide into sync. If the time difference is greater than 300 usec the ASD16HD will perform a time jump. (See *jump mode vs. glide mode*)

It is important to use a high quality GPS receiver with a stable output. If the 1PPS is jumping around in time the ASD16HDs outputs may glide back and forth or the outputs may also jump around as the result, simply because the generator is trying to track the pulse position.

Many high quality GPS receivers are able to suppress the 1PPS pulse if it is not reliable, only outputting the 1PPS when it is absolutely correct in time.

The ASD8V can fully accommodate this scheme. It only needs three consecutive 1PPS pulses to place the video frame correct. After these three pulses, the 1PPS is in principle no longer necessary. The generator will keep this correct position as long as the 10 MHz from the GPS receiver is available and stable.

Note: GPS 1PPS and some video formats have no useful timing relationship. Use only the 10 MHz/1PPS input when 1 second divided by the video frame rate is an integer number.

AES input

The AES input is AES/EBU and AES3id compatible, transformer balanced and terminated with 110 Ohms. The signal is evaluated for correct frame format, biphasic coding violations and out of frequency range before it is routed to the intelligent input detector. The incoming

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sample rate frequency is selected by the push buttons on the front panel.

Video outputs

The video sync outputs are available on six BNC connectors on the back panel. The outputs are individually buffered, 75 ohms and SMPTE/EBU standard amplitude when terminated. The signal is DC coupled with blanking level at zero Volts (black level). The video sync format is selected by the pushbuttons on the front panel. Sixteen different SD and HD formats are available (see Appendix for available formats). All components of the video sync signal are digitally synthesized from the same master clock, making the relationship between sync, sub carrier, luminance and chrominance fixed and temperature independent. Digital filters are employed on the individual components before they are summed to a composite video signal. Analog filters are used to remove any digital artifacts that may cause aliasing in digital video equipment. Slew rate limiting of the sync pulses is used for both SD and HD formats.

An undershoot limiter is placed right after the digital filters to prevent synchronization problems. The limiter level is preset to -1.5 IRE below black level.

Word outputs

The Word outputs are available on four BNC connectors on the back panel. The outputs are individually buffered, 75 ohms and TTL level.

The Word output frequency follows the chosen AES output sample rate frequency on the front panel, i.e. 44.1 kHz, 48 kHz or 96 kHz.

The rising edge of the word clock is aligned to the AES sub-frame A and the trailing edge is aligned to the AES sub-frame B. Thus a high level indicates left channel and a low level indicates right channel of the audio data.

AES outputs

The AES outputs are available on a 25 pin female D-sub connector, wired to the Yamaha standard. All AES outputs are individually buffered, 110 ohms, transformer balanced and 5V PP when terminated (full swing buffers). Further, an AES3id output on a BNC connector is available. The output is bipolar (no DC) 1 Volt pp into a 75 ohms load.

The output sample rate is selected by push buttons on the front panel. Available sample rates are 44.1 kHz, 48 kHz or 96 kHz.

AES special feature

Information about the selected Video sync output format is embedded in the AES signals user bits. The information is a one byte code, clocked in by eight consecutive word clocks, starting at the AES block boundary (see Appendix).

This code is aimed at equipment designers, as a tool to communicate information. It is of no practical use for the average user.

The AES outputs are intended for synchronization purposes and should ideally be empty of audio data to avoid build-up of clock and data jitter in the connected cable.

However, some commercially available AES receiver chips exhibit PLL lock problems when subjected to a "black" AES signal, producing an unstable and jittery master clock.

The problem is overcome by setting the first eight audio data bits to 1 and the remaining sixteen bits to 0. This gives a DC offset in the audio signal of -90 dBFS or approximately 0.2 mV with reference to +18 dBu.

A standard digital audio input circuit will easily accommodate this DC offset, and the scheme efficiently eliminates the lock problems.

AUX Outputs

The AUX outputs are basically identical to the Word output. The outputs are individually buffered, 75 ohms and TTL level.

The output frequency is the selected Word frequency multiplied by the factor listed on the front panel. The multiplication factor can be selected by push buttons on the front panel.

The CBL (Z-preamble) signal is aimed at system integrators and service personnel as a diagnostics tool, for delay testing, scope trigger or similar purposes. It is of no practical use for the average user.

Alarm output

The alarm output is 75 ohms, TTL level and active low. It is controlled by the intelligent input signal detector. The output reacts instantly and goes low when the input sync is lost. It reacts instantly again and goes high when the input signal returns or when control is handed over to the internal reference.

In case of a lost or an erratic sync, the flywheel will keep the sync running smoothly, but the alarm output provides the means to set up an early warning system, so the user will be warned of sync discontinuity problems before they become a problem.

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Mechanical and electrical specifications:

Dimensions : Width 19 inch, height 1U (44 mm), depth 220 mm

Weight : 5.5 kg

Power requirements : 180 - 240 VAC 50 Hz, 8 Watts (EU Version)

: 90 -120 VAC 60 Hz, 8 Watts (US Version)

Reference Inputs : Composite Video sync, 16 formats. SD bi-level sync, HD tri-level sync balanced, unterminated 10 kOhms, 0.15 -2.0 V PP (75 Ohms termination by switch)
: Clock input, 8 formats 10 kOhms, 0.5 V - 10 V PP, square or sine
: 1PPS clock, 10 kOhms, TTL level
: AES input, balanced 110 ohms 1.0 -5.0 V PP, 44.1, 48 and 96 kHz

Outputs : SD bi-level and HD tri-level video sync, 16 formats. 75 Ohms SMPTE/EBU level
: AES3 transformer balanced 110 ohms, 5 V PP into 110 Ohms, 44.1, 48 and 96 kHz
: AES3id single ended output, 1 volt PP bipolar into 75 ohms
: Word clock, 75 Ohms, TTL level, 44.1, 48 and 96 kHz
: AUX outputs, 8 formats, 75 Ohms, TTL level
: No-sync alarm. 75 Ohms. TTL level, active low.

Stability/accuracy : Oven crystal accuracy 0.2 ppm/25 deg. C, stability +/-0.2 ppm 0 - +50 deg.C
: Hue accuracy > 0.5 degrees, SD formats
: SC-H phase accuracy > 1 degrees, SD formats
: PLL capture range +/-25 ppm.
: PLL jitter video outputs < 1 nsec PP
: PLL jitter AES outputs < 1 nsec PP
: PLL jitter Word outputs < 1 nsec PP
: PLL wander video input/video output < 2 nsec PP
: PLL wander 10 MHz input/video output < 1 nsec PP
: PLL wander Word input/video output < 1nsec PP
: PLL wander AES input/video output < 1nsec PP

Appendix Detailed Technical Description

Position lock vs. frequency lock

The ASD16HD will perform a position lock between input and output whenever the mathematical relationship between the waveforms allows for it.

A position lock is not always possible. When this is the case, the ASD16HD performs a frequency lock.

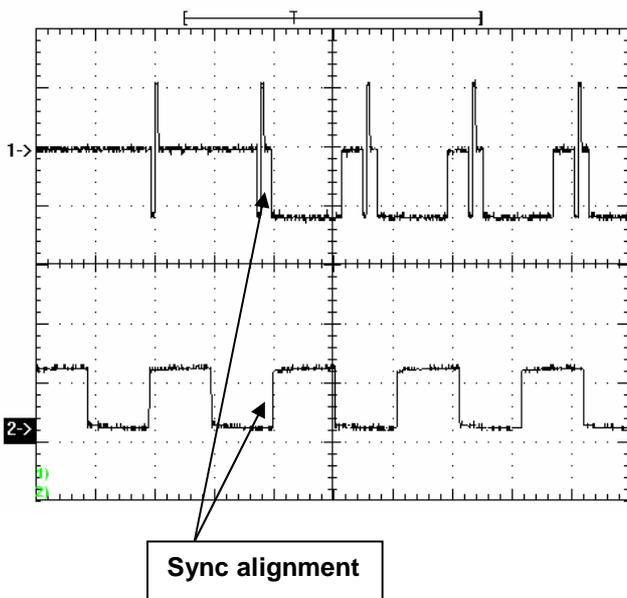
A good example of a frequency lock is a Word Sync input at 44.1 kHz synchronizing a 525 lines progressive scan video. The frame frequency is 59.94 Hz, giving 735.735735 Word pulses for every frame.

The ASD16HD does not give up on these two seemingly incompatible formats. It performs a mathematical calculation, finds a common denominator and performs a phase lock that will yield a perfect lock between the two frequencies.

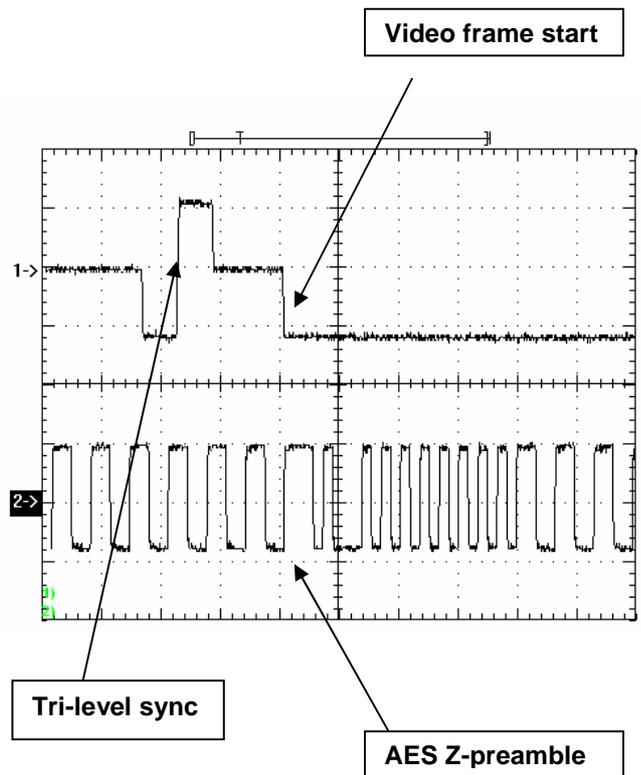
A typical *position* lock between two different formats can be seen on the scope snapshot below.

The incoming sync is a Word clock at 48 kHz (lower trace) and the output is a 1080i 25Hz HD Video (50 Hz frame frequency).

Note the precise alignment of the leading edge of the word and the frame start of the 1080i video. The ASD16HD calculates and applies the appropriate delay for correct sync alignment – *always!*



Below is an example of a position lock between an incoming AES at 48 kHz (lower trace) and an outgoing Video sync, 1080i 25Hz (50 Hz frame frequency). Note that the video frame start, following the tri-level sync pulse, is perfectly aligned with the AES Z-preamble start.



The AES recommendation states that the time difference between video frame start and AES block start should be less than 1 usec.

The ASD16HD aligns these start positions within one clock cycle at 27 MHz, i.e. less than 37 nsec.

The reason for this difference is simply component tolerances and variation in component parameters. The time difference is fixed. It does not wander and it does not jitter outside the specified performance parameters!

ASD16HD Reference Generator

Below is an example of a position lock between two different video formats.

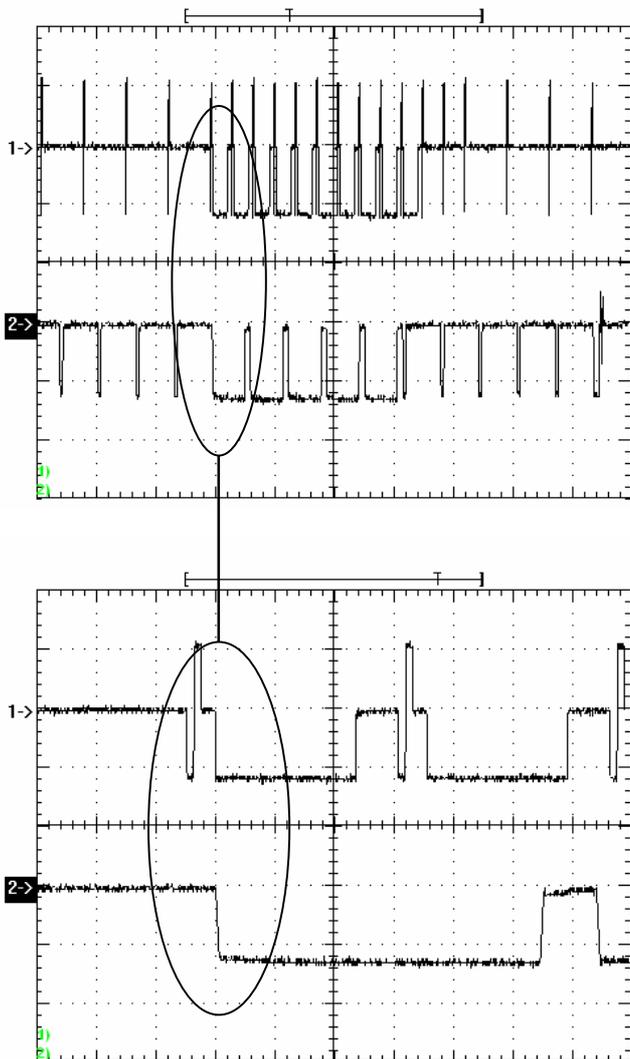
The incoming sync is a standard PAL B (lower trace) and the outgoing sync is a 1080i 25Hz (50 Hz frame frequency)

The frame start for the PAL and the frame start for the 1080i are perfectly aligned, although they have different line pulse frequencies, and thus different time intervals between their horizontal and vertical sync pulses.

A common mistake is to align the two videos by using the first sync pulse after frame start (vertical sync pulse). Typically this happens when low budget sync separators are used in the design.

The result is an incorrect position between the two frame starts when the two formats are different in line frequency, even though their frame rates are identical.

In such cases, the ASD16HD calculates and applies the necessary time delay as it always does, and the two frames are aligned correctly.



ASD16HD Reference Generator

Supported video formats:

Format	Interl/Prog, frame rate	SD/HD	Standard	AES user bits code
PAL B @ 25Hz	Interl, 50 Hz	SD		0000 0000
NTSC @ 29.97 Hz	Interl, 59,94 Hz	SD		0000 0010
525p @	Prog, 59,94 Hz	HD	BTA-1004, ITU-BT.1362	0000 0100
625p @	Prog, 50 Hz	HD	ITU-BT.1362	0000 1000
720p @	Prog, 60 Hz	HD	SMPTE 296M-1, 274M-2	0000 1010
720p @	Prog, 50 Hz	HD	SMPTE 296M-3	0000 1100
720p @	Prog, 30 Hz	HD	SMPTE 295M-4, 296M-5	0000 1110
720p @	Prog, 25 Hz	HD	SMPTE 296M-6	0001 0000
720p @	Prog, 24 Hz	HD	SMPTE 296M-7, 296M-8	0001 0010
1035i @ 60 Hz	Interl, 60 Hz	HD	SMPTE 240M	0001 0100
1080i @ 30 Hz	Interl, 60 Hz	HD	SMPTE 274M-4, 274M-5	0001 1010
1080i @ 25 Hz	Interl, 50 Hz	HD	SMPTE 274M-6	0001 1100
1080p @ 30 Hz	Prog, 30 Hz	HD	SMPTE 274M-7, 274M-8	0001 1110
1080p @25 Hz	Prog, 25 Hz	HD	SMPTE 274M-9	0010 0000
1080p @ 24 Hz	Prog, 24 Hz	HD	SMPTE 274M-10, 274M-11	0010 0010
1080Psf @ 24 Hz	Prog, 48 Hz	HD	ITU-R-BT.709-5	0010 0100

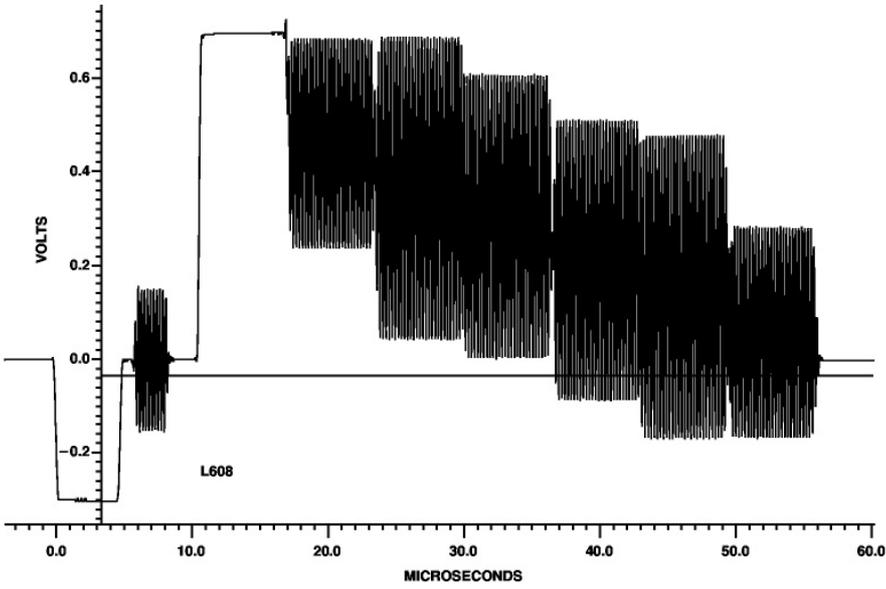
ASD16HD Reference Generator

Relationship between video output and AES/Word/AUX outputs

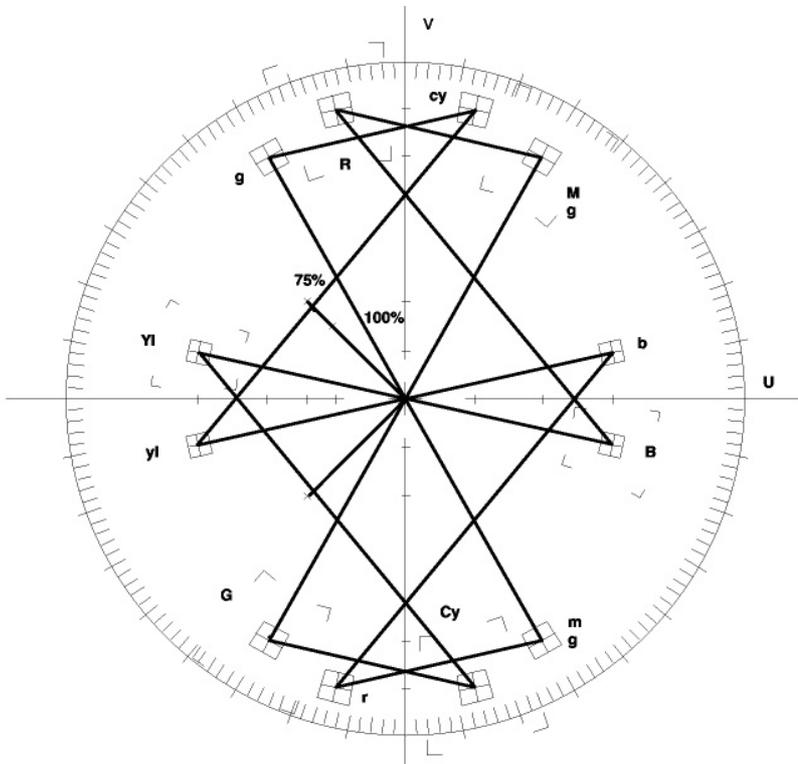
VIDEO SETTING		AES, 44.1k	AES, 48k	AES, 96k	Word 44.1k	Word 48k	Word 96k	CBL @ 48 and 96	Clk x 2	Clk x 4	Clk x 8	Clk x 32	Clk x 64	Clk x 128	Clk x 256	OUTPUT
PAL, 25	⌘															
NTSC, 29.97	⌘															
525p, 59.94	⌘															
625p, 50	⌘															
720p, 60	⌘															
720p, 50	⌘															
720p, 30	⌘															
720p, 25	⌘															
720p, 24	⌘															
1035i, 60	⌘															
1080i, 30	⌘															
1080i, 25	⌘															
1080p, 30	⌘															
1080p, 25	⌘															
1080p, 24	⌘															
1080Psf, 24	⌘															

Legend: Position Lock Frequency Lock

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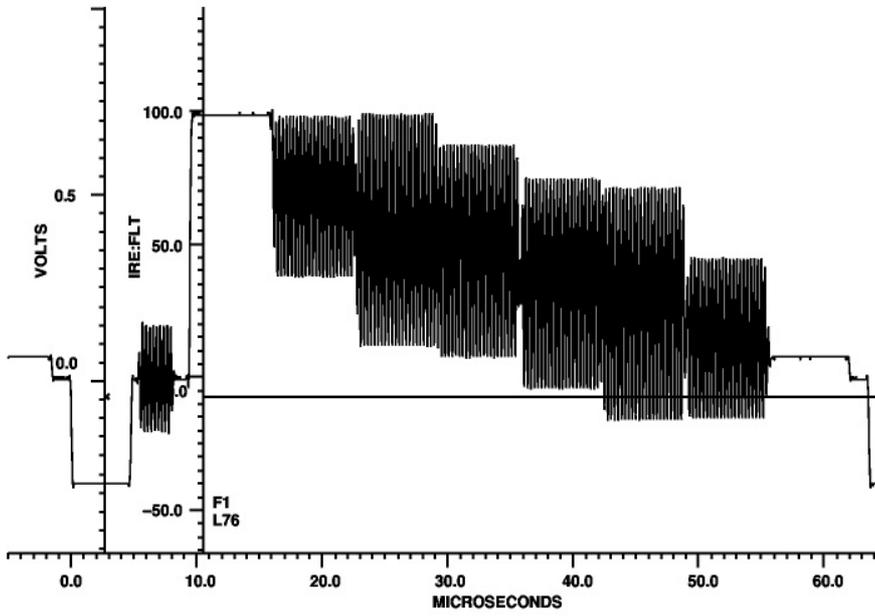
100/75 EBU PAL Colorbar



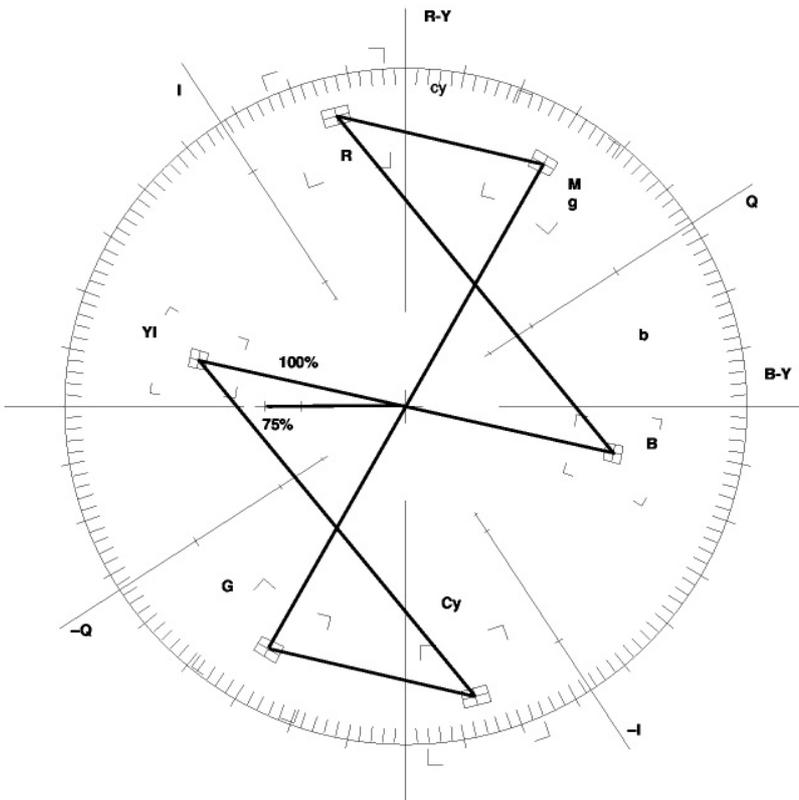
PAL vector plot

ASD16HD Reference Generator

100/7,5/75/7,5 NTSC Colorbar



NTSC vector plot



ASD16HD Reference Generator

PLL Jitter and Wander measurements

The jitter measurements were performed by locking the ASD16HD to various incoming sync sources and measuring the resulting jitter and wander specifications at the outputs. The output signal was read out by a digital storage oscilloscope while triggering on the incoming sync source. The oscilloscope was set to infinite persistence

Note that this method is brutally revealing. Many manufacturers specify jitter in a most favorable way, just to get to print impressive specification on their PR material. These figures are often misleading, and they are often without relevance to the requirements of the real world.

When specifying jitter as RMS, the manufacturer is hiding behind the fact that the relationship between the RMS measurement and the peak-to-peak measurement largely depends on the spectral characteristics of the noise (and hence jitter) in the circuit. In case of a pure thermal noise source, the factor can be as low as 2.8. In case of an electronic circuit, which generates both thermal noise and a lot of flicker noise, the factor can easily reach 8-10. That way a manufacturer can specify for example 2nsec jitter as 200 psec jitter!

Another way of fooling the customer is to apply bandwidth limitation to the measurement. One of the worst despicable and misleading ways is to specify jitter in the audio band, from 20 Hz to 20 kHz only. The bandwidth of the circuits used in the generating of sync signal is normally 60 – 80 MHz and the flicker noise and hence jitter is produced in the entire frequency band of the electronic circuit.

This little PR trick will reduce the data sheet jitter figures substantially, in severe cases up to 50 times!

Another neat little trick is to specify the main oscillators RMS jitter. This figure is often advertised to be 6-8 psec RMS, which is actually pretty normal for most budget oscillators. Anyone can buy this for a couple of dollars. The figure has absolutely no relevance; it just looks good on paper. It is a specification of a single circuit element in a long chain of signal processing elements.

The specification that matters is the resulting output jitter, measured as peak-to-peak, at the output terminals of the unit! In the modern HD video world, video and audio are sampled, multiplexed and transmitted at clock speeds ranging from 270 MHz to above 1.5 GHz. ALL the jitter that is generated by a device should be specified in peak-to-peak figures, in order to judge the possibility of sampling errors and thus degradation of the program material being transmitted.

Measurement on the ASD16HD was performed the following way:

Jitter was measured at full bandwidth, DC to 100 MHz. The DC condition reveals wander in phase locked loops.

Jitter was measured Peak to Peak. All the generated jitter components are contained in this measurement.

The ASD16HD was allowed to warm up for 10 minutes to enable the master oscillator to fully stabilize.

The PLL was allowed to maintain lock for 1 minute in order to settle before the measurement started.

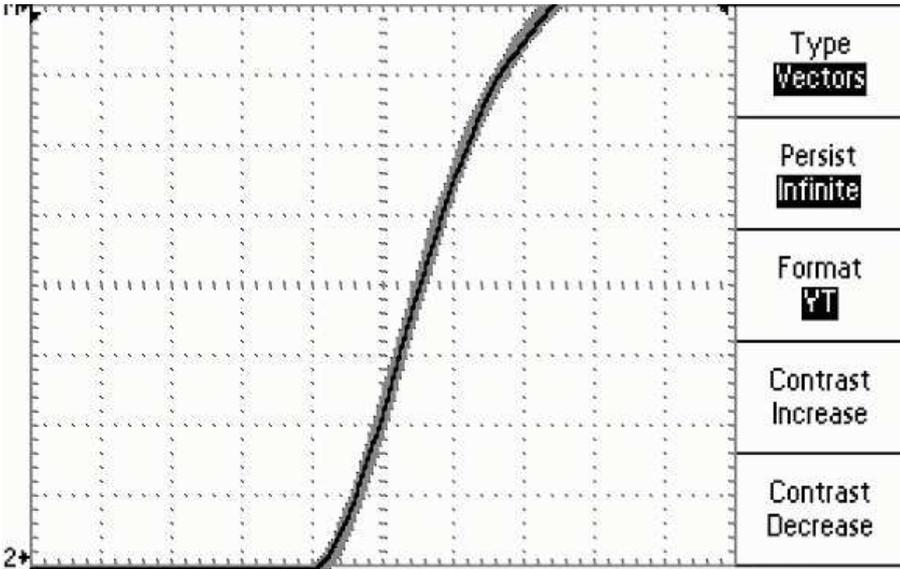
The measurement time was 5 minutes continuously for each graph.

The persistence of the scope was set to infinite. Thus the grayed out area represent the total sum of *jitter+wander* accumulated over the time of the measurement.

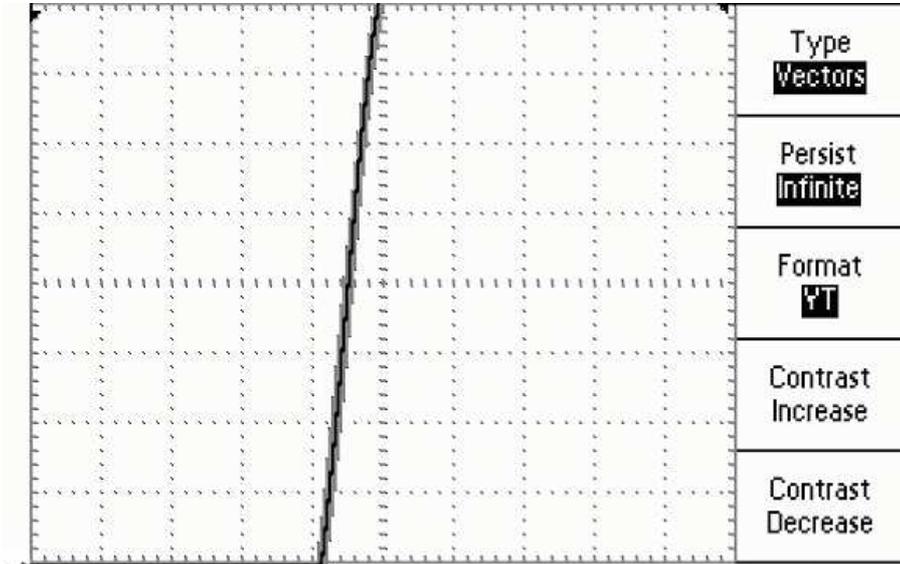
The actual horizontal position of the graph is not relevant for the measurement. It was simply chosen to be at a place with a clear view. The results can be seen on the following scope screen dumps.

The sum of jitter+wander is less than 1.5 nsec PP for video/video and less than 1 nsec PP for all other configurations.

ASD16HD Reference Generator

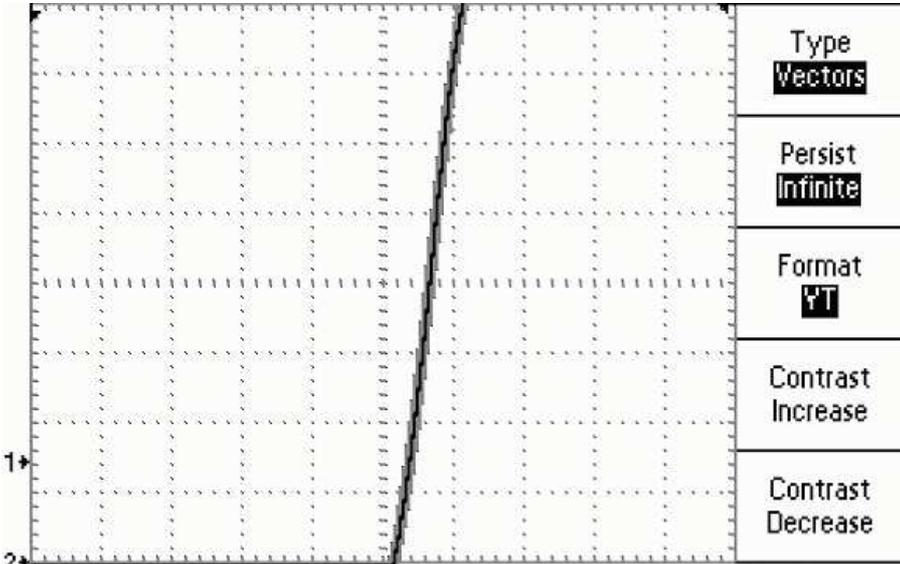


PLL Jitter and Wander. Video in/ Video out. 5nsec per div

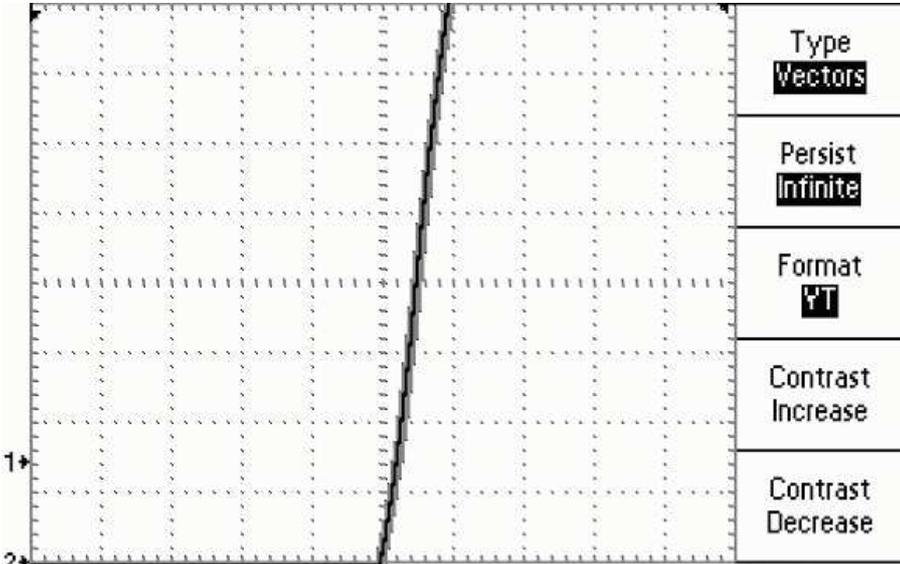


PLL Jitter and Wander. 10 MHz in/ Video out. 5 nsec pr div

ASD16HD Reference Generator

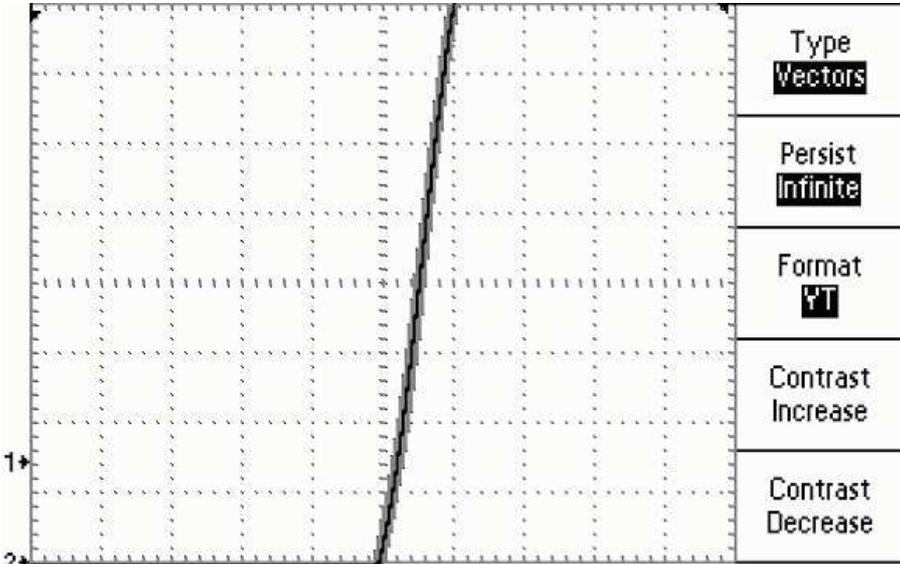


PLL Jitter and Wander. AES 48 kHz in/ Video out. 5 nsec pr div

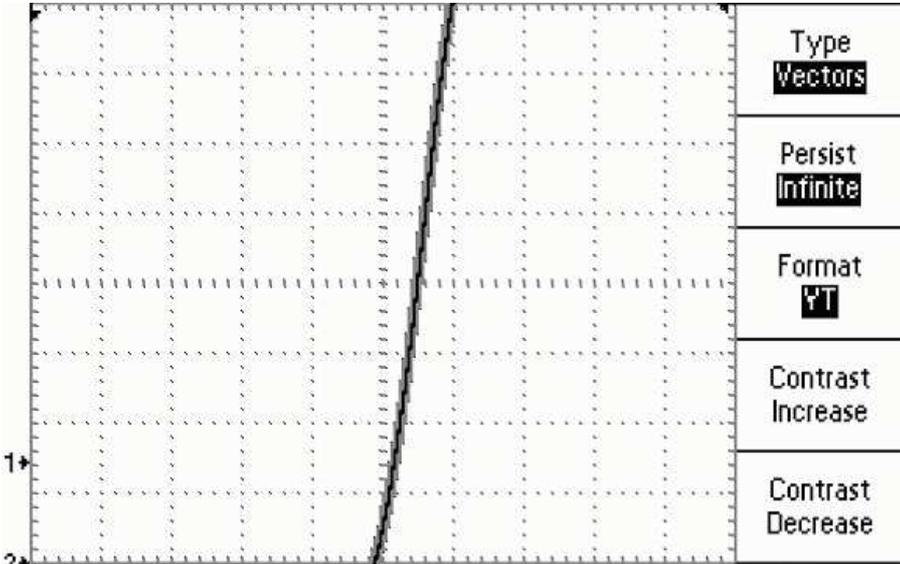


PLL Jitter and Wander. AES 44.1 kHz in/ Video out. 5 nsec pr div

ASD16HD Reference Generator

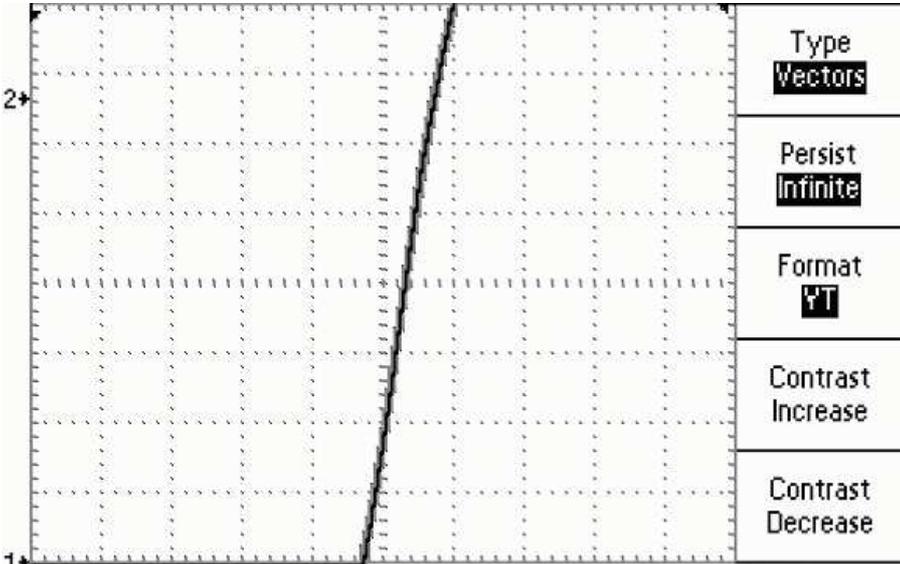


PLL Jitter and Wander. Word 48 kHz in/ Video out. 5 nsec pr div



PLL Jitter and Wander. Word 44.1 kHz in/ Video out. 5 nsec pr div

ASD16HD Reference Generator



PLL Jitter and Wander. Video out/AES 48 out. 5 nsec pr div

ASD16HD Reference Generator

Relationship 1PPS, Video, Word and AES

