

Balanced inputs with auto threshold detector, 50% slicing and noise/jitter rejection.

The input circuit detects the "sweet spot" of the incoming sync in order to reject ringing and noise jitter created by incorrect termination or incorrect cable impedances.

Even a wildly ringing and noisy signal is cleaned and pulse shaped into a virtually perfect output signal.

The input is able to accept from 10V to 0.2V signal level which means it will accept AES3, AESid, S/PDIF and TTL/CMOS levels.

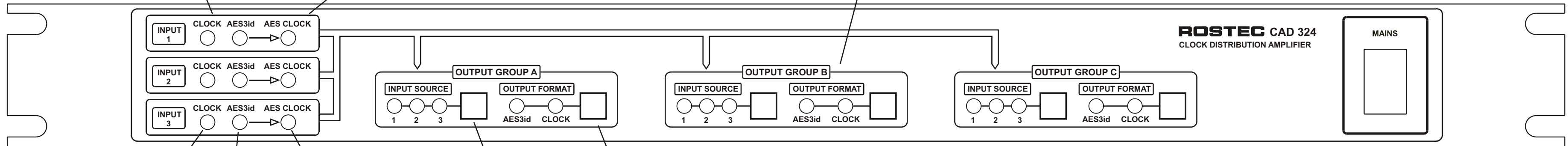
The input circuit automatically detects whether a clock signal or an AES signal is applied to the input. When a valid and correctly formatted AES signal is detected, the Word clock is extracted from the AES stream and will be available for distribution through the output buffers. The choice of Word clock or AES3id output is made on each individual output buffer group by a pushbutton.

The input accepts clocks up to 24.576 MHz and AES11/AES3/AES3id and S/PDIF at 8kHz - 192 kHz sample rates. The Word clock can be extracted from the AES stream at 32kHz - 108 kHz sample rates. The extracted Word clock jitter is typically less than 50pS RMS. Note that when a S/PDIF signal is applied, the status bits in the digital stream will continue to be at consumer status. The output will be AES3id level and the extracted clock will be TTL level.

Each output group can be assigned to any input. The output level can be set to standard TTL (0- 5V) for word clocks, super clock, GPS etc. Or it can be set to bipolar 1.2V pp into 75 Ohms for ASD3id

The long-haul output buffers are able to drive 100 m cable

Individual power supplies for each output group ensures no crosstalk jitter or crosstalk noise between groups when different frequencies or formats are used



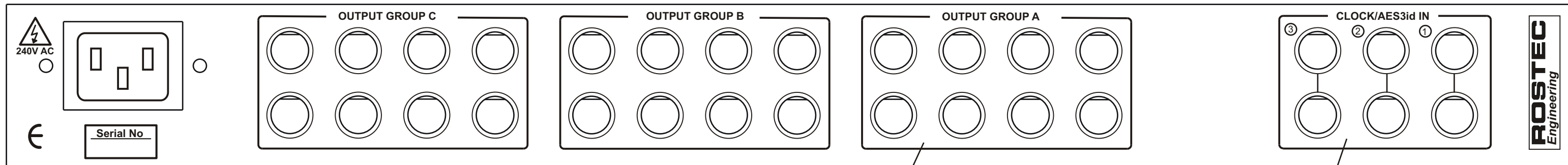
Indicates that a clock is present at the input

Indicates that a valid AES/AES3id or S/PDIF is present at the input

Indicates that the Word clock is successfully extracted from the AES/AES3id or S/PDIF signal

This pushbutton selects the input source

This pushbutton selects the output format



Each group features 8 individual 75 Ohms long/haul buffers and separate power supply

The Inputs are high impedance balanced buffers with internal loop-thru for serial connection of additional units.

The inputs are highly sensitive and fully overload protected and accept levels from 0.2 Volts to 10 Volts.

The overall bandwidth is DC to 25 Mhz, making the unit suitable for all relevant clock frequencies, ranging from 1PPS to Pro-tools super clock

The excellent ASD3id transfer characteristics supports any format from 8kHz to 192kHz sampling frequency