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ADA432 AES Distribution Amplifier

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Contents

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Features

- 4 inputs into 32 outputs (4 groups of 8)
- Transformer balanced inputs and outputs
- True balanced architecture.
- The Inputs have "sweet spot" detectors, providing auto-slicing and signal clean-up.
- Inputs accepts from 0.2 to 10V
- High speed. Supports sampling frequencies from 30 kHz to 400 kHz. The bit depth is not relevant.
- Outputs are full swing buffers, 5 Volts PP into 110 ohms, 10 V PP open.
- Latency from input to output is less than 50 nsec
- Yamaha Standard pin-out on 25pin D-SUB
- Separate power supplies for inputs and for each output group.
- Linear low noise power supplies.
- Short circuit proof. Self protecting. Individual thermal protecting for each output group.
- Inputs and outputs are ESD protected to 23 kV, IEC 61000-4-2 and 15 A surge, IEC 61000-4-5
- 19" sturdy steel metal casing
- Affordable price

General description

The ADA432 is a high quality AES distribution amplifier designed to operate in a broadcast, video or audio studio installation. It has 4 inputs and 32 outputs configured as 4 groups of 8 outputs. Any of the 4 output groups can be freely selected to connect to any of the 4 inputs. The input accepts AES, AES3 and SPDIF levels.

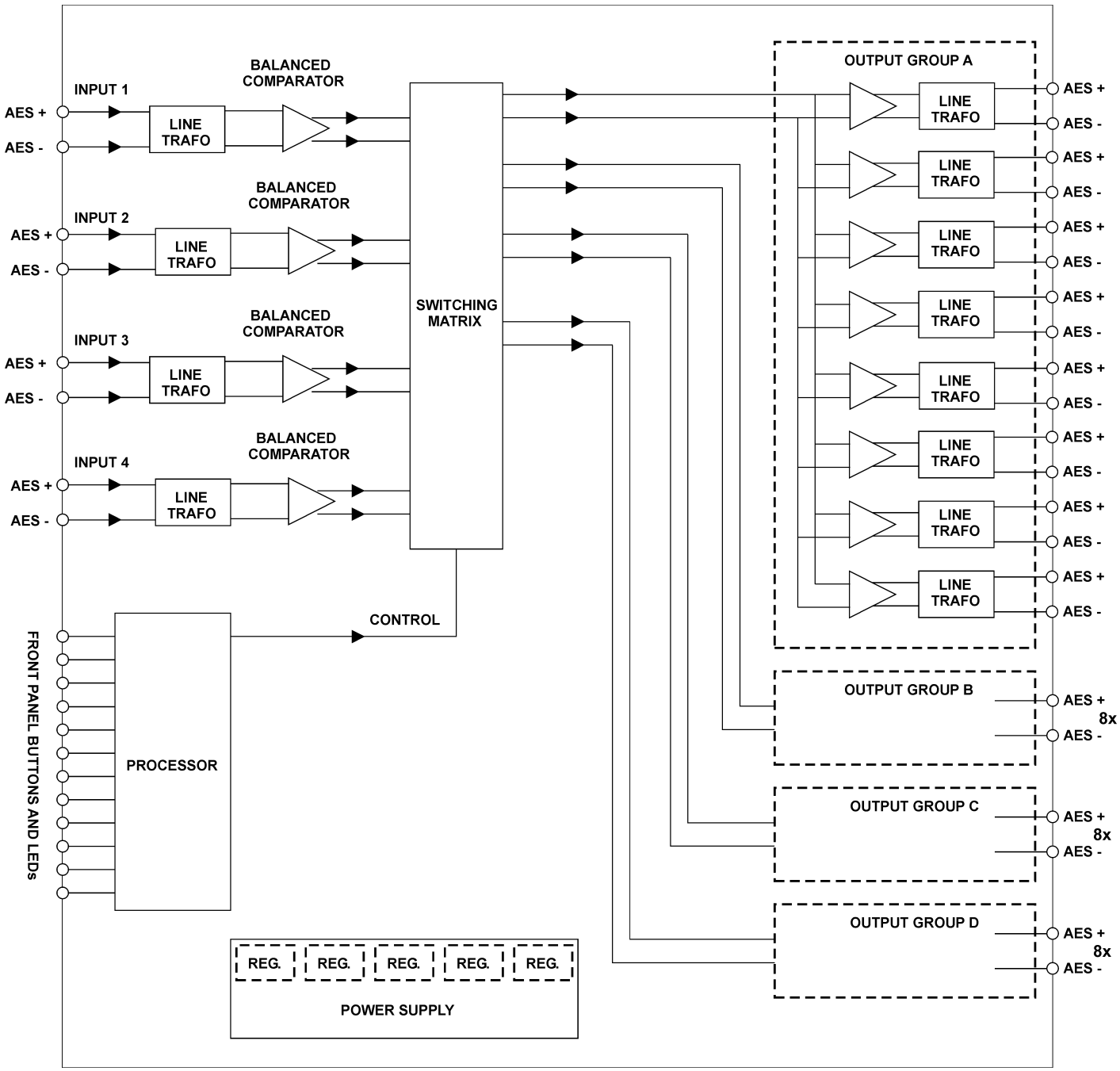
The ADA432 features an internally true balanced architecture. All inputs and outputs are fully floating transformer balanced and individually buffered. The input and output circuits are state of the art, resulting in an impressive 40 MHz overall bandwidth, and a latency from any input to any output of less than 50 nsec. Sampling rates from 30 kHz to 400 kHz are supported.

The input circuit and each of the 4 output groups have their own individual power supply. The separate power supplies and the overall balanced architecture effectively creates an efficient isolation barrier between groups, thus eliminating crosstalk and jitter transfer when different sampling frequencies and different data structures are distributed through the same unit.

Each of the inputs features a discrete high-speed comparator with hysteresis and a "sweet spot" detector, which performs an accurate auto-slicing of the input. This means that the circuit automatically chooses the most useful part of the input signal, thus being able to clean-up and reconstruct a ringing and noisy input signal into a perfect output signal.

The 32 individual output buffers are high speed and transformer balanced. The output level is 5 Volts into 110 ohms (10V no load).
And the output buffers are fast! The rise time of the output pulse is less than 8 nsec with an overshoot of less than 2%.
The fast rise time makes the output signal appear well defined and clear cut seen from a standard AES receivers point of view. This enables the receiver to react to the signal with maximum accuracy and minimal jitter.

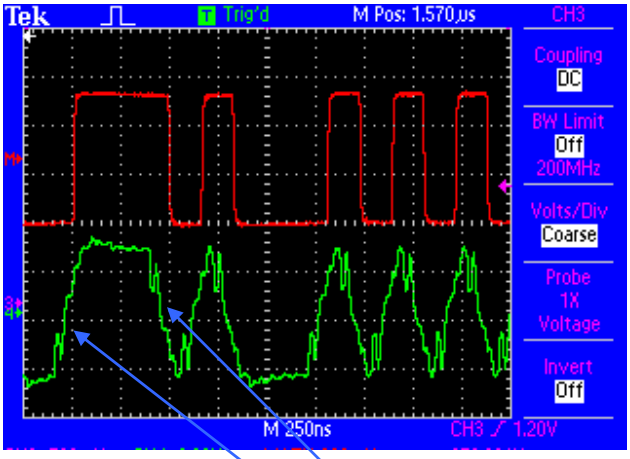
Simplified Functional Schematic



Input circuit

Each input circuit consists of a discrete balanced high speed comparator. The signal from the input transformer is fed balanced into the comparator, in order to reject any common mode noise and spikes that are transferred across the transformer by parasitic capacitances. This configuration is able to establish the trigger point with great accuracy, with a dramatically improved jitter response as a result.
The input circuit also features a "sweet spot" detector, which detects ringing and HF noise and performs auto slicing, which always places the trigger point inside the healthiest zone of the input signal.

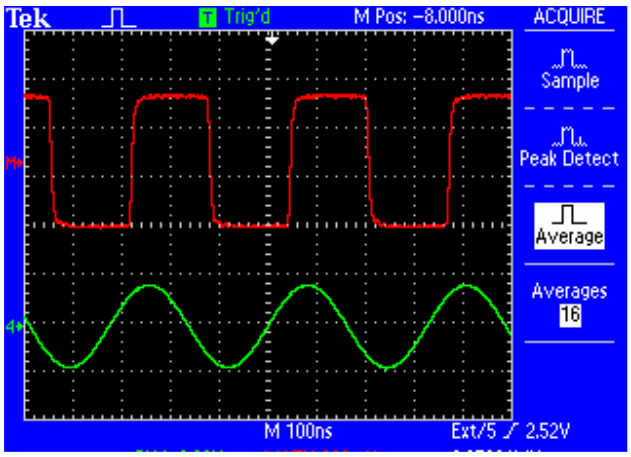
The mechanism is able to regenerate a wildly distorted input signal into a clear-cut perfect output signal.
The oscilloscope snapshot below illustrates this clearly. The lower trace is an input signal with lots of noise and ringing, possibly due to wrong termination, incorrect cable impedance or faulty grounding.
The upper trace is the reconstructed signal measured at the output.



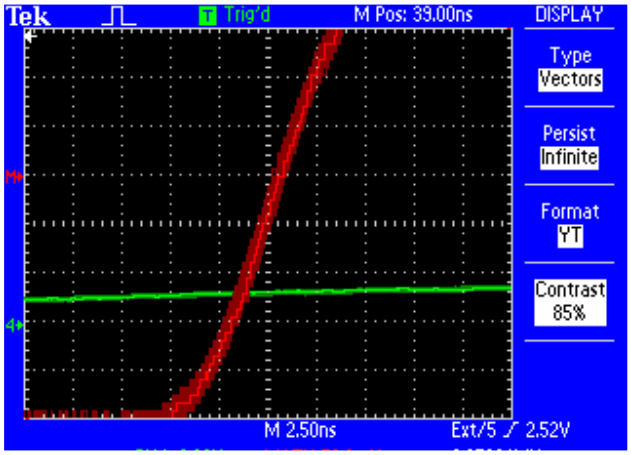
Auto slicing

The signal is an AES at 48 kHz sampling rate. The time scale is 250 nsec/div. The measurement bandwidth is 200 MHz.

The next scope snapshot illustrates the excellent noise characteristic of the input. A sine wave at the data clock frequency of a 48 kHz AES signal is used. A sine wave is used because it represents the slowest rise time at a given frequency, i.e. the signal stays the longest time in the trigger zone. Hence it represents the greatest challenge for the input comparator circuit.



Correct auto slicing gives a perfect duty cycle

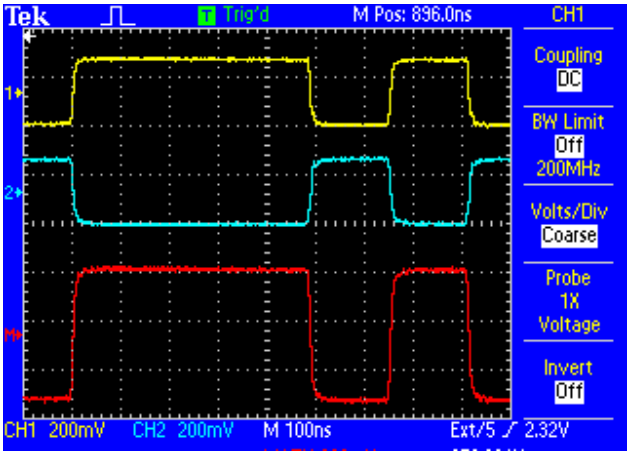


Extreme jitter test with sine wave

Notice on the upper snapshot how the auto slicing circuit faithfully generates a 50/50 duty cycle square wave at the output.
On the lower snapshot, a closer look at the output reveals that the slow moving sine wave (green trace) triggers the output with extremely little jitter. Persistence of the scope was set to infinity, the measurement time was 2 minutes and the measurement bandwidth was DC to 200 MHz. *Harsh conditions indeed!*
The result is excellent: Approx. 1 nsec peak to peak, which equals less than 150 psec RMS of jitter.

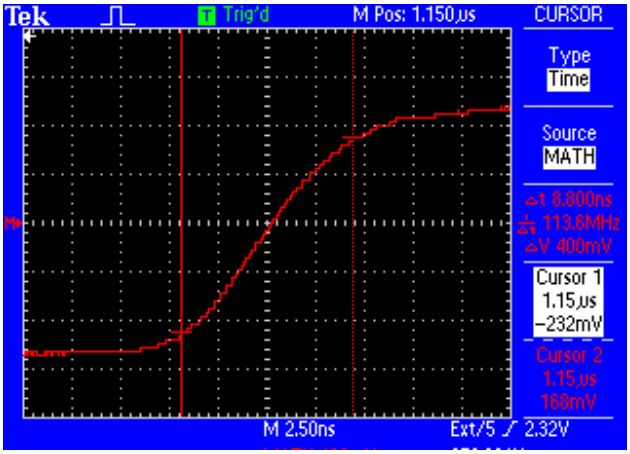
Output buffers

The output buffers are differential buffers, meaning that they drive the output transformers in a balanced mode. The common mode accuracy and high speed of these buffers minimizes transmission of switching transients through parasitic capacitances to the output.
The result is freely floating clean balanced outputs with symmetrical rise and fall times.



Excellent output balance

The above scope snapshot shows a measurement taken across a free floating 110 ohms load at the end of 3 m audio cable of good quality. Two 10 Mohms/16 pF probes was used.
The two upper traces are the positive and negative output, and the lower trace is the output result. The outputs are beautifully well balanced even though they are in fact floating freely.



Fast rise time

The output buffers are fast! In fact the whole unit is fast! The scope snapshot shows a rise time of a little less than 9 nsec. The rise time is measured between 10 % and 90 % of the leading edge. This equals a bandwidth of approx. 44 MHz.

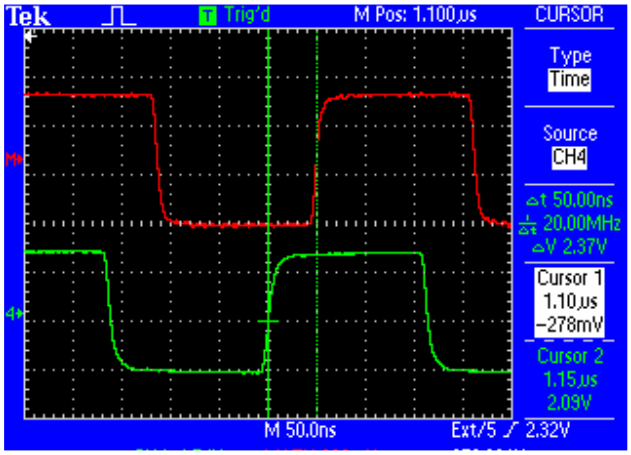
As the fastest clock in the AES signal is 64 times the sampling frequency, it follows that the fastest useable sampling frequency of the device is 688 kHz.

Well, it hasn't been tested - yet!

Switching matrix

The switching system is just a balanced cross-point switch, connecting the inputs to the outputs according to the settings on the front panel.
The switch is controlled by the system microprocessor, and the settings are saved immediately in non-volatile memory when changes are made on the front panel. Instant memory!

Latency (delay)



50 nsec latency

The above scope snapshot shows the total time delay through the unit, from input terminal to output terminal. The lower trace is the input. The upper trace is the output. The signal is an AES at 48 kHz sample rate. One 0 and 1 of the bit stream are shown.
The total delay from input to output is 50 nsec.

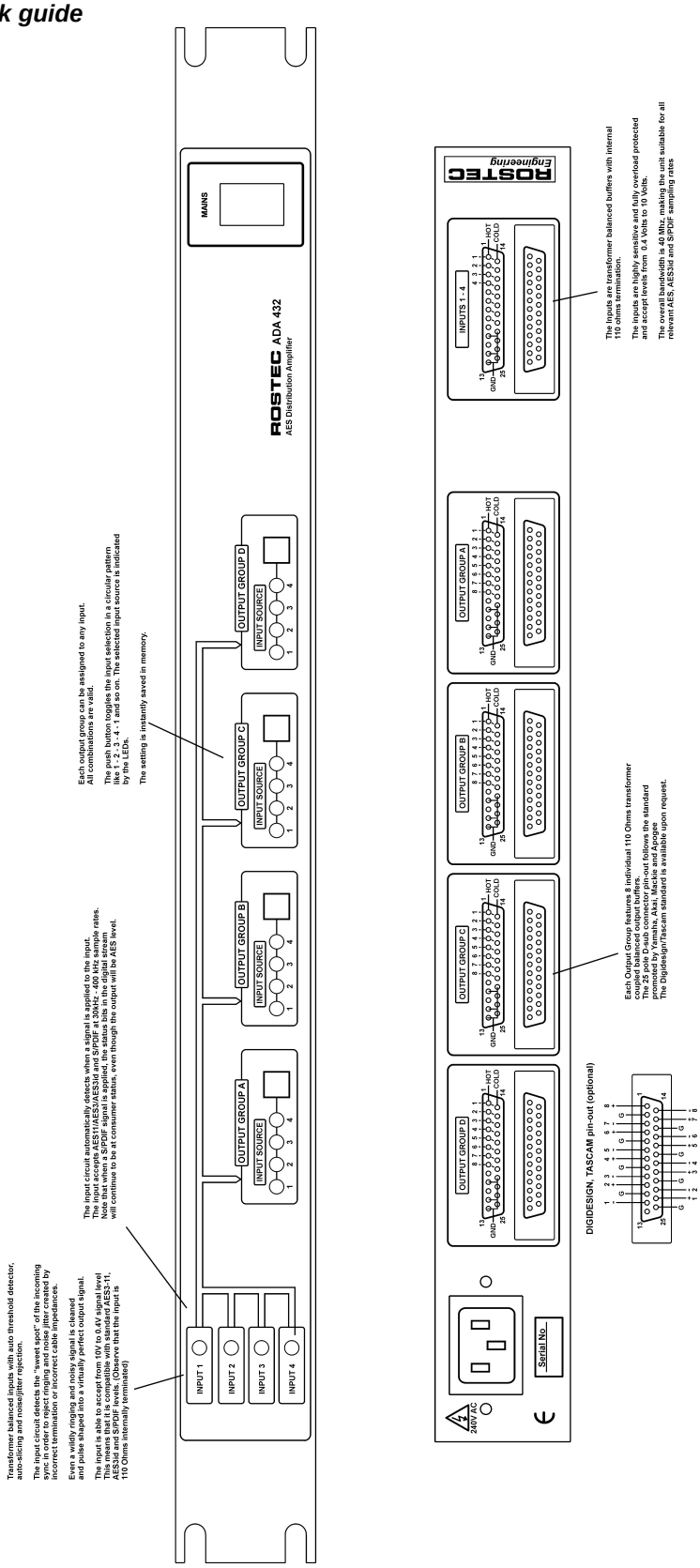
Power supply

The unit has 5 separate power supplies. One for the input section and one for each of the output groups. Each group has separate ground planes as well. The separation ensures that ground currents and supply transients cannot cross between the groups.

This configuration is essential for low jitter specifications. When different sampling frequencies and different data structures are distributed via the 4 output groups, crosstalk will invariably create data jitter. The independent power supplies and the separate ground planes together with the balanced architecture have efficiently eliminated this problem.

To further maintain the excellent jitter and low noise specifications, the unit is equipped with a toroidal mains transformer and a high quality mains input filter.

Front and back panel quick guide



Mechanical and electrical specifications:

Dimensions	: Width 19 inch, height 1U (44 mm), depth 150 mm
Weight	: 3.0 kg
Power	: 180 - 240 VAC 50 Hz, 8 Watts (EU Version)
	: 90 -120 VAC 60 Hz, 8 Watts (US Version)
Inputs	: Number of: 4
	: AES input, transformer balanced, 110 ohms, 0.2 -10 Volts PP
	: compatible with AES3-11, AES3id and S/PDIF levels
	: ESD protected to 23 kV, IEC 61000-4-2 and 15 A surge, IEC 61000-4-5
Outputs	: Number of: 32
	: Configuration: 4 groups of 8 outputs
	: AES3-11 outputs, transformer balanced, 5 volts PP into 110 ohm, 10 Volts open.
	: ESD protected to 23 kV, IEC 61000-4-2 and 15 A surge, IEC 61000-4-5
Environment	: 0 - +50 deg C operating
	: 0 - +70 deg C storage